## Remarks

Applicant respectfully requests reconsideration of this application as amended. Claims 19, 25, and 28 have been amended. No claims have been cancelled. Therefore, claims 19-37 are present for examination.

Claims 19-22, 24-31, and 33-36 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Anderson (U.S. 5,905,910) and Jones et al. (U.S. 5,619,723).

Applicant respectfully submits that the present claims are patentable over the combination of Anderson and Jones. Anderson discloses a system for the simultaneous operation of multiple disk drives in a computer. The system includes a first disk drive having an interrupt generating circuit to generate a first interrupt signal. The first disk drive receives a first disk transfer command from the computer, processes the first disk transfer command, and generates the first interrupt signal upon completion of the first disk data transfer command. See Anderson at col. 1, ll. 49-56.

The system also includes a second disk drive, also having an interrupt generating circuit to generate a second interrupt signal. The second disk drive receives a second disk transfer command from the computer while the first disk drive is processing the first disk transfer command such that both the first and second disk drives are simultaneously active. The second disk drive processes the second disk transfer command and generates the second interrupt signal upon completion of the second disk data transfer command. See Anderson at col. 1, ll. 56-65.

Moreover, the Examiner has admitted that, "Anderson fails to specifically teach an interface connected to the system bus and receiving requests from the BIOS." See Office Action dated June 14, 2002 at page 4 lines 3 and 4. Applicant further submits that

Jones does not disclose or suggest an interface connected to the system bus and that receives requests from the BIOS.

Jones discloses a disk drive array (DDA) controller. The controller includes a microcontroller CPU with embedded ROM and RAM, a bus interface, and five connected disk drives. The ROM 104 contains the firmware for controller. A system bus coupled to the bus interface provides a communication link between the controller and a host computer, which uses the array of disk drives as secondary memory. See Jones at col. 14, ll. 18-27. When the host sends a read or write request to the array via the system bus, the interface translates the request to the controller, which generates access requests for each of the individual disk drives. See Jones at col. 15, ll. 10-15. The DDA controller sends all disk drive requests, and not the host computer. See Jones at col. 15, ll. 13-16.

Claim 19 recites, a Basic Input/Output System (BIOS), a system bus coupled to the BIOS, and an interface coupled to the system bus that receives disk drive requests from the BIOS via the system bus. Thus, for Jones to teach the present invention, the BIOS must be connected to the system bus and send disk drive requests to the interface over the system bus. Jones does not teach or suggest such a configuration.

The Examiner asserts that, "Jones discloses an interface connected to a system bus and communication with the BIOS." See Office Action dated June 14, 2002 at page 4 lines 8 and 9. As support for this assertion, the Examiner cites Fig. 1; Col. 14, Lines 24-31; and, Col. 23, Lines 15-25. A careful review of these three citations will demonstrate that Jones does not teach or suggest the configuration of the present invention.

First, Figure 1 shows a system bus 109 connected to a bus interface 108. However, Figure 1 does not show a BIOS connected to the system bus 109 that is

connected to the bus interface 108. Thus, Jones does not teach or suggest a BIOS in communication with the interface. Further, column 14, lines 24-31 does not mention a BIOS. Instead, a ROM that exists on the Disk Drive Array (DDA) controller is described. This controller, with its ROM, is positioned after the interface, and is not connected to the system bus.

In addition, column 23, Line 15 is a section that describes the DDA controller. The DDA controller comprises a microcontroller CPU shown in Figure 1 by numerals 102, 104, and 106. See Jones Col. 14, Lines 18-15. The BIOS that the Examiner refers to in the office action is contained in the ROM, numeral 104. See Jones Col. 23, Lines 16 and 17. Thus, the BIOS is connected to the interface and not to the system bus.

In sum, Jones teaches a system bus connected to an interface and an interface connected to a BIOS. This configuration is not the same as a BIOS connected to the system bus and a system bus connected to an interface. Without the BIOS, described in Jones, being connected to the system bus, the BIOS cannot transmit disk drive requests on the system bus, and the interface cannot receive disk drive requests from the BIOS via the system bus. Therefore, Jones does not teach or suggest an interface connected to the system bus and receiving requests from the BIOS.

As the Examiner admits, Anderson does not teach the limitation of an interface connected to the system bus and receiving requests from the BIOS via the system bus. Also, as shown above, Jones does not teach the limitation either. Therefore, since neither Anderson nor Jones teaches the invention as claimed, any combination of Anderson and Jones cannot render the claims obvious.

Further, combining Anderson and Jones teaches a system that is both inoperative and illogical. The combination yields a system where a BIOS is connected to a system bus that is then connected to an interface. Then the interface is connected to another BIOS, and finally to the striper and the disk drives. There is no need to have two BIOS in the system. Accordingly, the combination of Jones and Anderson does not teach the present invention. Therefore, applicant respectfully submits that claim 19 is patentable over any combination of Anderson and Jones.

Claims 20-22 and 24 depend from claim 19 and include additional limitations. As a result, claims 20-22 and 24 are also patentable over the combination of Anderson and Jones.

Claim 25 recites transmitting an IDE request from a Basic Input/Output System (BIOS) onto a system bus and receiving the IDE request at an IDE interface connect to the same system bus. Therefore, for the reasons stated above with respect to claim 19, claim 25 is also patentable over the combination of Anderson and Jones. Since claim 26 depends from claim 25 and includes additional limitations, claim 26 is also patentable over the combination of Anderson and Jones.

Claim 28 recites an interface coupled to a system bus that receives disk drive requests from a Basic Input/Output System (BIOS). Accordingly, for the reasons stated above with respect to claim 19, claim 28 is also patentable over the combination of Anderson and Jones. Because claims 29-31 and 33-34 depend from claim 28 and include additional limitations, claims 29-34 are also patentable over the combination of Anderson and Jones.

Claim 35 recites a Basic Input/Output System (BIOS) and an IDE interface coupled to the system bus where IDE requests from a Basic Input/Output System (BIOS) are received by the IDE interface via the system bus. Thus, for the reasons stated above with respect to claim 19, claim 35 is also patentable over the combination of Anderson and Jones. Since claim 36 depends from claim 35 and includes additional limitations, claims 36 is also patentable over the combination of Anderson and Jones.

Claims 23 and 32 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Anderson (U.S. 5,905,910) and Jones et al. (U.S. 5,619,723) and further in view of Jenkins (U.S. 4,047,157).

Applicant submits that the present claims are patentable over Anderson and Jones even in view of Jenkins. Jenkins discloses a controller in a secondary storage facility that can transfer data from a recording medium over either of two independent buses in a data system. See Jenkins at col. 2, ll. 36-40. Nevertheless, Jenkins does not disclose or suggest an BIOS coupled to a system bus that transmits disk drive requests to an interface via the system bus. As described above, neither Anderson nor Jones disclose or suggest such a limitation. Therefore, the present claims are patentable in view of any combination of Anderson, Jones and Jenkins since none of the references disclose or suggest an BIOS coupled to a system bus that sends disk drive requests to an interface via the system bus.

Claim 37 stands rejected under 35 U.S.C. §103(a) as being unpatentable over Anderson (U.S. 5,905,910) and Jones et al. (U.S. 5,619,723) and further in view of Mizuno et al. (U.S. 5,608,891).

Mizuno discloses an array type recording system that divides a single circuit into a write circuit and a read circuit. See Mizuno at col. 4, ll. 30-35. However, Mizuno does not disclose or suggest an BIOS coupled to a system bus that sends disk drive requests to an interface via the system bus. As described above, neither Anderson nor Jones disclose or suggest such a limitation. Therefore, the present claims are patentable over any combination of Anderson, Jones and Mizuno.

Applicant respectfully submits that the rejections have been overcome, and that the claims as amended are in condition for allowance. Accordingly, applicant respectfully requests the rejections be withdrawn and the claims as amended be allowed.

The Examiner is requested to call the undersigned at (303) 740-1980 if there remains any issue with allowance of the case.

Please charge any shortage to our Deposit Account No. 02-2666.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

Date: 8/12/02

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Marked Version to Show Changes Made
Insertions are underlined, deletions bracketed.

19. (Thrice Amended) A system comprising:

[an interface coupled to a system bus that receives disk drive requests from] a Basic Input/ Output System (BIOS);

a system bus coupled to said BIOS [via the system bus];

an interface coupled to said system bus that receives disk drive requests from said BIOS via said system bus;

a striping controller coupled to said [between the interface and the first and second disk drives, that causes data being transmitted between the system bus and the first and second drives to be written to and read from the first and second drives in an interleaved form and substantially in parallel];

a first disk drive coupled to said striping controller; and,

a second disk drive coupled to said striping controller, said [the] first and said second disk drives each having data separator electronics, data formatting electronics and head positioning electronics; and

said striping controller causes data being transmitted between said interface and said first and second drives to be written to and read from the first and second drives in an interleaved form and substantially in parallel.

25. (Amended) A method comprising:

[receiving] transmitting an IDE request from a Basic Input/ Output System (BIOS) [at an IDE interface via] onto a system bus; [and]

receiving said IDE request at an IDE interface connected to said system bus;

writing to and reading from a first disk drive and a second disk drive in an interleaved form and substantially in parallel in response to [the] said IDE request.

28. (Thrice Amended) A striping disk controller comprising:

an interface coupled to a system bus that receives disk drive requests from a Basic Input/ Output System (BIOS) separately coupled to [via the] said system bus; and

control logic coupled to the interface to cause data being transmitted via the system bus to be written to and read from a first disk drive and a second disk drive in an interleaved form and substantially in parallel.